Antares: A Synergy between University Education and Research, Development and Technology Innovation Groups

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Abstract – Although Education and other activities related with Research, Development and technological Innovation (R+D+I) are all integrated by the Universities, their typical organization leads to a low coupling among them. In this way, R+D+I activities are usually carried out by small elitist groups with a high degree of external self-funding. The activities of the above groups are leaded by professors and also are directly related with postgraduate Education (mainly Ph .D. but also Ms. Sc. in a less degree). On the other side, undergraduate education, also carried out by the above professors, generally is poorly connected with their R+D+I activities. Therefore, one of the most difficult tasks in an University Department is to make compatible its educational purpose with its innovation activity performed through the research and the development activities of its research groups.

In this article we report on a successful experience about a close cooperation of the above activities within an University Department which has leaded to the design of the Antares platform suitable for educational purposes on microprocessors as well as for R+D+I activities carried out by one of the research groups of the Department. The synergy due to the above situation opens new opportunities for further cooperation among Education and (R+D+I) activities.

I. Introduction

The *Departamento de Ingeniería Electrónica* of the *Universidad Politécnica de Madrid* is a University Department composed by 28 Professors, 5 Technicians and 3 Administratives. It leads teaching duties in the *Escuela Técnica Superior de Ingenieros de Telecomunicación* and it maintains several R+D+I lines in parallel with its education activity, one of them oriented to embedded systems. The common point of convergence for the educational and the R+D+I activities described here is the study and design of microprocessor-based systems. The educational activities of the above Department in this field and within the 5 year career of the *Ingeniero de Telecomunicación*, comprise the following set of undergraduate subjects: a theoretical one in the 3rd year, (*SEDG: Sistemas Electrónicos Digitales*) together with a practical laboratory also in the 3rd year (*LSED: Laboratorio de Sistemas Electrónicos Digitales*), just following the former. There is also an advanced theoretical subject (*ISEL: Ingeniería de Sistemas Electrónicos)* and a second laboratory (*LSEL: Laboratoio de Sistemas Electrónicos*) both in the 5th year of the career. All the above subjects are related with microprocessor systems and one of our main goals was how to approach with continuity and complementariness the above subjects in order to have coherent stages in the formative process of our *Ingeniero de Telecomunicación*, and how to connect our students with our R+D+I activities on embedded systems. All the above would give them an education in the state of the art, although it would require some modern equipment for the above

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laboratories. If a synergy of the above objectives was obtained, the formation received by our undergraduated students would be a high quality one, taking advantage of the real experience and dedication of the professors, and other experienced people which could also include the R+D+I staff.

In our previous *64M2 educational* plan which has been active until few years ago, the subjects of the 3rd and 5th courses about microprocessors were performed on two different microprocessor systems, offering a vision about the two dominant microprocessor families in those years: Motorola and Intel. However, the diversity of architectures available in the market at this moment does not clearly support this approach. The high capabilities of today's processors (both in processing power and in the integrated peripherals they have), their low price, the wide use of high-level languages for their programming and the free distribution software tools easily available, have changed drastically the panorama. Today it is possible, and sometimes preferable, to use a single platform able to offer different perspectives of systems based on microprocessors and microcontrollers, both at a basic level (without an operating system, working directly on the microprocessor and its peripherals), as well as at a high level (on the basis of an operating system supporting application developments and device drivers).

Recently our Department received some funding to bring up-to-date the equipment of its 3rd year Laboratory about microprocessors, within the framework of the recent *P-94* educational plan. One possibility was to buy some standard microprocessor development boards but we decided to design our own system instead, using the experience on the subject of the LSI group, a R+D+I group within our Department, LSI coming from *Laboratorio de Sistemas Integrados*. The result is the Antares platform, a microprocessor development board based on the powerful MC5272 integrated system, being used by the LSI group for its R+D+I activities. The above platform not only serves perfectly for the 3rd year Laboratory subject, but also it fits very well in the more advanced 5th year Laboratory due to its performances, peripherals and communication capabilities, thus saving equipment costs. Therefore, the theoretical subject in 3rd course has been modified accordingly to give the proper support and the necessary basis for the new platform.

II. Educational Laboratories

The practical education and training on microprocessor based systems is given to our students through the *Laboratorio de Sistemas Electrónicos Dgitales* and the *Laboratorio de Sistemas Electrónicos*.

II.I Laboratorio de Sistemas Electrónicos Digitales

The *Laboratorio de Sistemas Electrónicos Digitales* (LSED) is a crowded laboratory, attending about 400 students per year. The students have to design, build, test and document a complete microprocessor-based system (both HW and SW) organized in groups of two people.

The starting point is a written description of the system to be implemented, with an extension of about 30 pages. It includes the functional specifications and requirements of the system (scope, general description and the scenarios of usability), part of the system analysis (system block description and a detailed description of the main subsystems) and both system and block implementation guidelines (modularity and a proposed SW base architecture that includes task distribution techniques among the main process and sub-processes, making special emphasis on the use of interruptions).

Starting from the proposed specification, the student must perform the complete analysis of the system (the initial specification is always incomplete and partially inconsistent) and to make its design, implementation, test and documentation. The target system changes every year and the

student must develop a completely functional prototype with its associated documentation, passing an individualized oral examination.

The evaluation of each student is performed in two steps: the first one is a continuous evaluation through the presentation of intermediate deliverables (helping Professors to verify the evolution and originality of the work), and the second one is the final examination using the complete documentation of the system and an oral examination (the Professors verify that the prototype fits the initial specifications and formulate individualized questions to determine the capacity of each student to explain the obtained results, degree of participation, etc.).

The approach we follow for this laboratory is to show the students not only the microprocessor capabilities and implementation technologies (the main objective) but the systemic point of view were systems are a multidisciplinary works (microprocessors and programming are the tools to build systems including communications, signal processing, mathematical operations, controlling, telemetry, user interfaces, etc.).

An important point covered by this laboratory is the management of real time components. The proposed approach to learn about these components is the use of routines that attend periodic interruptions, although it complicates both system debugging and the development of the prototype. To help students, some recommendations are provided in the initial description about how to face the problem of the real time, mainly the concurrence and the resource sharing [3].

Taking into account these general guidelines, this is a laboratory oriented to design a complete system (open to the students creativity and encouraging them to reach their own solutions), with a systemic character and close related to the design of simplified (as far as possible, both economically as time demanding) consumer systems, partially guided (orienting to teach the students how to organize the different laboratory sessions to reach the objectives in a professional-like environment) and with a high emphasis on the creativity and the professionalism of each group of students (to reach the maximum mark, the students must implement optional improvements on the basic proposed system, supposing more than a 15% of the total, or afford the design of an special practice). Other factors like the technical writing quality, the skills for oral communication, group working capabilities, etc. are also individually valued.

This laboratory is closely connected with its corresponding theoretical subject (*Sistemas Electrónicos Digitales SEDG*), previously studied, and centered in the same microprocessor and peripherals. Both subjects try to balance a high formative content both in the basic knowledge and the system design with an accessible workload.

II.II Laboratorio de Sistemas Electrónicos

The *Laboratorio de Sistemas Electrónicos* takes place on the second semester of the 5th year and has a non mandatory character within the specialty of *Electronics*. The first consequences of these facts are the small number of students, about 20, allowing us to afford a personalized training and evaluation of each student.

The main objective of this laboratory is to design from scratch a complete electronic system applying the same methodology as used in industrial environments and covering the different tasks from the marketing or sales engineering to the industrialization, passing from the research and development engineering. It includes the following aspects:

- Design methodology.
- System specification from vendor to the engineering department.
- Design and validation strategies for complex systems.

- System characterization and test.
- Documentation, including user manuals, and technology transfer.

Secondary goals are to stimulate the student's creativity and initiative, introduce them to the methodologies used on professional engineering teams, and act as a bridge between the previously studied subjects within an academic approach and their professional career as productive engineers.

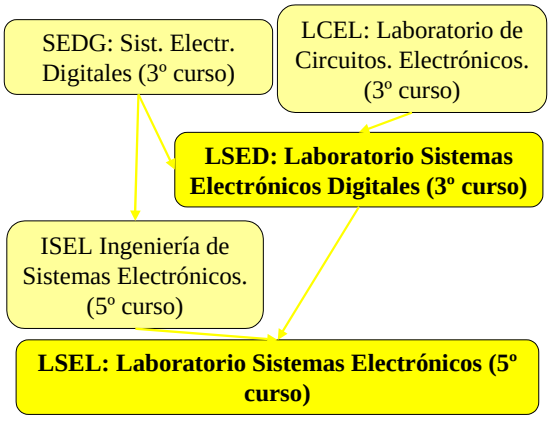
As time and effort to be applied by the students to this laboratory is limited, we have moved from the programming in assembler used in the *Laboratorio de Sistemas Electrónicos Dgitales* to high level programming, module reusability, the use of a *Linux* operating system and the extensive use of *Internet* for the acquisition of building blocks.

The natural evolution of the students that follow this laboratory is to use the performed work as a base for their *Proyecto Fin de Carrera*. With this scope on mind, the creativity, novelty and functionality of the platform are an essential requirement.

To cover the described scenarios, we have specified some generic base platforms the students use to develop the system. These basic general purpose basic platforms are tuned to communication applications and include a wide variety of communication interfaces of and the possibility of adapting them to new technologies.

Before the development of the *Antares* platform and its educational version (*DAntares*), the platforms have been used on this laboratory, based on microprocessors Motorola 68000, 68HC11 and 68331 did not support the development of ambitious practices [2] because of the low performances on processing capabilities, memory and peripherals.

As an example, a system including speech synthesis or recognition, with these platforms (with included a low capacity in non-volatile memory to store the voice patterns and samples) only allowed audio processing with a bandwidth of 2 KHz, very far from reality.



III. *Antares*: The need for a common basic plattform

The LSI know how in the design of embedded systems, its disposition for the cooperation in the graduate education and the effort of a group of Professors of the *Departamento de Ingeniería Electrónica* led to the creation of a working group to design of a new platform, *Antares*.

The design of the new platform has been focused to fulfill a set of specifications, some essential and other advisable to maximize its use both for education and research and development

activities. One of the basic requirements for the platform was to use a state-of-the-art technology in order to support professional and advanced developments. With this approach it is possible to get a better student motivation, it guarantees its application in research, development and technology transfer projects and prepares the students to face real professional systems of immediate implantation on the market.

Other important restriction was the necessity of taking the complete control on the platform design to be able to use it in industrial research and development projects and to include improvements and modifications when needed, some of them results of the students work.

Along the last years it has been a meteoric advance in telecommunication technologies, with a proliferation of new communication networks, both for short distance (Bluetooth, WLAN, ICM, PLC, etc.), and for long distance (GSM/GPRS, UMTS, ADSL, satellite, etc.), which is specially suited for the development and use of embedded systems. To address the development of student practices on telecontrol and telemetry over the new communication networks, the platform must be able to support these new technologies and include the possibility of Internet access by supporting a wide variety of physical networks and being able to accede and provide services over the TCP/IP protocols.

Once settled the objective of designing an embedded system development platform we can list the main characteristics that differentiate them from the general purpose computers:

- **Price:** One of the most important constraints in the design of embedded systems is the final price per unit. These equipments are usually fabricated in large quantities (tens of thousands units) and thus, this factor becomes a fundamental parameter to be considered in the design. To achieve this objective, application tuned platforms using slow clock microprocessors and minimizing the built-in memory are mandatory. In general, these systems do not include an operating system, although we can also find enlightened ones if flexibility is needed, due to the hardware limitations. In our platform we have opted to include an operating system to gain in flexibility and reduction on the students design effort.
- **Power consumption:** This is another important factor to consider at the design time because most equipments are battery powered.
- **Size:** As in the case of power consumption, most embedded equipments are portable or have an important restriction in size.

The base platform has been used in Laboratorio de Sistemas Electrónicos for the last year is based on PC-104 equipment with Linux operating system, and including libraries and tools for rapid prototyping. Nevertheless, these platforms are very expensive and prone to crash on non trained hands, as the student ones, which makes the yearly supporting cost rather expensive.

According to hardware, the educational platform must be generic enough to allow the development of a wide range of applications without adding external hardware, and provide powerful connections to add specific hardware as needed.

To provide flexibility it has to include an operating system allowing the applications to access the different hardware resources, as memory or communication ports, provide a file handling system and to support multitasking. The desired characteristics of an operating system for an embedded system are:

- **Reliability**: Main consideration is its robustness and dependability; it has not to fail under any circumstances.
- **Multitasking:** It is common to find in the embedded systems several synchronized tasks running at the same time, whose implementation is much simpler if the operating system supports multitasking. These kinds of operating systems automatically manage the hardware resources allowing all the tasks to use the same resource without interferences among them.
- **Oriented to communications:** As previously settled, the main area of applications is the development of embedded equipments over the new communication networks, thus it is necessary that the operating system supports the widest number of facilities on this field (TCP/IP, PPP, Bluetooth, etc.).
- **Easy hardware control:** It must provide support for the complete and hierarchical control of the platform hardware.

Considering that the first students contact with this platform in within the third year, with a low level of experience on circuitry, it is mandatory to provide it with a set of protections to allow the daily work without damaging the base hardware and an easy maintenance of the equipment. Finally, it is advisable to provide the student with well known interfaces that allows an easy integration of additional hardware elements, as serial and parallel ports or analog inputs and outputs.

The main conclusion when analyzing the platform design requirements is the necessity of developing two printed circuit boards, a first one with the complete system functionality and another one with the protections.

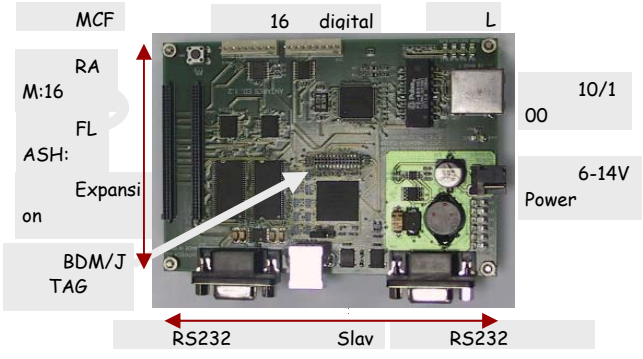
IV. *Antares*: Description of the generic plattform

This point describes the base board hardware and briefly summarizes the selected solutions when more than one design alternatives exist. The name we have chosen for the base platform is *Antares*t.

Antares is build around the Motorola *Coldfire* family of microcontrollers, and uses the M5272C3 because its suitability for communications. The general features of *Antares* are the following ones:

- Motorola 32 bit microprocessor MCF5272
- SDRAM memory: 16 MBytes
- Flash memory: 4 MBytes
- Ethernet interface
- Two RS-232 serial ports
- USB slave interface
- BDM/JTAG interface for debugging and direct Flash memory program
- Eight digital LCMOS outputs
- Eight digital LCMOS input/outputs
- Four general purpose signaling LED
- Complete Motorola expansion bus access
- Switching power supply accepting DC input voltages from 8-14 Volts.

The picture shows the *Antares* platform with its size and the different modules location. The board has a high integration density, on a 10 layer PCB, which allows a high degree of compactness, 12cm × 9cm.



Next points describe in detail the different modules.

IV.I Microprocessor

For *Antares* it has been selected the Motorola *Coldfire* MCF5272 microcontroller attending three main reasons, its performances for the development of communication oriented embedded systems, the Linux support and the compatibility with the old 68000 microprocessors wich allows a non dramatic transition in the educational subjects.

The *Coldfire* is a 32 bit microcontroller, evolution of the 68000 family, oriented to the embedded systems market, and is the Motorola strategy to address these applications for the next years. It is a 32 bit RISC microprocessor with variable instruction length. With instructions of 16, 32, or 48 bits, the generated code is more compact than the obtained in the classic 32 or 64 bits RISC architectures. This feature allows a more efficient memory usage and a bandwidth reduction in the instruction reading cycle, what increases the global performances of the system and reduces the amount of needed memory.

Another *Coldfire* advantage is its compatibility with the 68000 family, allowing an easy program migration between them, which is very convenient to migrate from the old 68000 based platforms applications to *Antares*, and specially the different in house developed tools for helping the Professors.

Motorola uses for the *Coldfire* family a different strategy to the general purpose microprocessors customers, as Intel or AMD, where the main effort to get better performances is to increase the clock frequency. The *Coldfire* approach is to develop a set of different chips around the microprocessor core that are tuned to fit families of applications by the inclusion of different peripherals.

Among all the models, available at the board development time, in the *Coldfire* family, we selected the MCF5272 because it integrates on a single chip all the communication peripherals that we wanted for our platform, including interfaces as Ethernet or SPI. This communications capability makes this microcontroller the most indicated for applications oriented to Internet, telephony on networks, LAN, WLAN, etc.

IV.II MEMORY

The memories selection, type and organization, for the platform are as important as the microprocessor and have a high impact on the system performance.

The platform integrates SDRAM memory and uses the internal controller included in the MCF5272. It incorporates two MT48LC4M1A2 SDRAM memory modules parallel connected to create a 32 bits bus, and allowing a total of 16 MBytes of RAM memory.

The platform also includes Flash memory for non nonvolatile storage and support two configurations with one or two memory banks of 2 MBytes, which ends with a total of 2 or 4 MBytes on board.

IV.I Interfaces

In an embedded systems development platform with the requirements we have previously stated, the communication capability and the interaction with external devices play a fundamental role, and imposes the integration of multiple communication interfaces.

In addition to the general communication interfaces as Ethernet, RS232 and USB, suited for connecting external standard devices and Motorola specific interfaces and bus to connect external chips, we have also included digital and analog input/outputs to allow the platform to interface external heterogeneous devices. The Motorola expansion bus available in a connector is very important because it allows the expansion of the platform by connecting external boards.

The Ethernet interface is built in two parts, the controller, integrated on the MCF5272, in charge of accessing the shared medium (MAC), and external hardware that performs the physical level functions, the voltage level conversion transformer and the twisted pair RJ-45 connector.

Antares also includes a BDM/JTAG interface to speed up the application debugging on the platform and minimizing the necessity of simulators, usually very expensive. The selection of the interface to use (BDM or JTAG) is done through a jumper.

The *Antares* expansion bus interface consists on two parallel connectors with the entire externally available MCF5272 chip signals to allow a full flexibility in board expansion with new hardware.

IV.III Power supply

Antares uses, when fed from mains, any external power supply from 220/125V AC to 8-14V DC and an output current higher than 200mA. This output is transformed to the internal board voltages 5V and 3.3V by a switching regulator for maximum efficiency.

V. *Dantares*: *Antares* oriented to a basic education

For a development platform, to successfully face a massive laboratory with students that are have not a high degree of practical skills in electronic systems, the inclusion of strong and reliable protections and robust mechanics is of vital importance. If properly designed and maintainability has been considered, also helps to lower the annual maintenance cost and to maximize the availability of the equipments throughout the students working time.

To cover this objective, and based on the previous experience of the Professors team in building “student proof” protections, like the 68000, 68HC11 and 68331 systems [2], we decided protect the externally available analog and digital inputs and outputs against overvoltages and shortcircuits, the most frequent actions in an educational laboratory.

Although a redesign of the *Antares* PCB was considered, we decided to build a separate protection board on which Antares is piggy backed via the expansion bus. This approach allows covering the complete spectrum from the student’s microprocessor initiation (fully protected) to the advanced embedded system design. The protection board also includes a 220V AC power supply, a mechanical box and receives the name of *DAntares*.

Opposite to the *Antares* requisites of minimum power consumption and size, to face the design of the protection board we only considered the robustness and maintainability of the equipment. It contains a linear 220V AC to DC power supply instead of a switching one for robustness, the protection circuitry has been design with no power consumption restrictions to increase the protected input/outputs bandwidth, a large set of LED has been included as informative visual interface for application debugging, etc.

Starting from the *Antares* platform, the protection board provides to the outside world, and as additional functionality for education purposes, two analog inputs and one analog output connected through the Motorola synchronous peripheral interface SPI, extends up to 32 the number of input/output pins, three interruption inputs, one timing input, three PWM inputs and one timed output. All these signals are optocoupled and buffered, allowing a bandwidth of 100 Ksamples/sec.

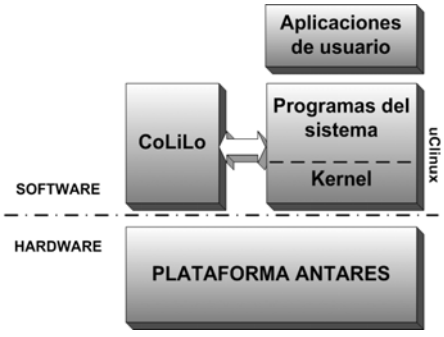
Analog input and outputs use 12 bit converters with track-and-hold controlled via the Motorola serial synchronous bus QSPI, the chips are the MAX1246 for the inputs and the MAX5352 for the outputs. The protection is provided by the HCPL7840 isolation amplifier with more than 50 KHz of bandwidth. Digital inputs/outputs are protected by HCPL2631 isolation high speed optocouplers.

The mechanical aspects are of special relevance in a board for massive inexpert usage. The box is metallic with a polycarbonate upper part for visibility; the connectors are female DB-25 and DB-9 for the digital signals and BNC for the analog ones. All connectors have been selected for their high robustness and standardization.

VI. Application development software for *Antares*

This part of the paper briefly describes the software used in *DAntares*, both external and in house developed. Software architecture is shown in the following figure.

On top of hardware is placed *CoLiLo*, the operating system charger, whose function is to initialize the hardware and to install the operating system. Next step is covered by the selected operating system, *µCLinux*, divided in kernel and system programs. The highest level is covered by the user applications. In parallel we can find the tools used for the development software. The following points briefly describe the different parts.



VI.I CoLiLo

The functions of this software are to configure the platform hardware and to recover a *µCLinux* distribution image which is stores on the Flash memory. We have started from the *CoLiLo* source code, initially developed by Rob Scott under GNU license, performing the necessary modifications to adapt it to the *Antares* hardware. New functionalities to test the hardware modules correct operation of and the possibility of charging different *µCLinux* images have also been added.

VI.II µCLinux

*µCLinu*x is an adaptation of the *Linux* operating system to work on microprocessors without memory management unit (MMU), as in the MCF5272 case. This operating system is smaller than standard *Linux* distribution, what makes it very suitable for embedded systems.

Kernel size, including the most common options, is below 500 KBytes and the complete distribution (Kernel plus applications) is below 900 KBytes. As with *Linux* distributions, the code is open, allowing a complete access to the operating system source code. This is one of its best advantages for education, and not only for education, because it is possible to take full control over the entire design.

Another strong point for the use of *µCLinu*x is that it is based on a *Linux* kernel, sharing all its advantages as: multitasking operating system, modular architecture, multiple network protocols support (TCP/IP, PPP, SLIP, etc., support for multiple file systems as NFS, Ext2, FAT32, FAT16, etc.), robustness and reliability, availability of the source code, as distributed under GNU license it is free, the software control of the hardware is very easy, etc.

It is possible to find *µCLinu*x distributions for a large number of microprocessors, including the Motorola *Coldfire* family. The *µCLinux* distribution is composed by three well differentiated

software blocks: the kernel, based on the version 2.4.x. we have modified to adapt the standard distribution to the *Antares* platform; the standard C library (*libc*) and its implementation for microcontrollers and finally the applications. The *µCLinux* distribution integrates different applications both for the system (i.e.: the command interpreter) and for the user applications (i.e.: a Web server).

These three blocks compose the system base software. The most relevant modifications have been performed on the standard *µCLinux* distribution to adapt it to the *Antares* hardware are the following ones: Flash memory controllers, SDRAM memory controllers, the development of specific controllers for several hardware interfaces and the file system support.

VI.III Development tools

The software development station is composed by a PC with a *Linux* distribution installed. This standard platform with free software allows the students to work at home and not necessarily in the laboratory, increasing its usage ratio. To help the programmer we have created a developer toolkit that includes a cross compiler, a cross debugger and a lot of useful tools which allows the user to also develop applications in a platform different from the *Antares* one.

The second tool for development is the BDI2000, a device that allows software debugging using the GNU debugger via the *Antares* BDM interface. This tool allows the user, among other possibilities, to write directly on the Flash memory, trace the content of the microprocessor registers, execute programs step by step, etc.

VII. A free application development toolkit for *DAntares*

Although it is possible to find in the market high quality development environments for the *ColdFire* (i.e. Metroworks), the license prices and special cables for program loading and debugging through the BDM interface are unaffordable for a massive usage in the laboratories. On the other hand, the actual free tools based on GNU-*Linux* are not intuitive enough to be used by students with little experience in system programming.

As results of teaching several years around Motorola microprocessors, we have developed for them two graphic frameworks running on Windows, both including an editor, an assembler and a debugger, and a complete set of manuals and practices for teaching students.

We have selected one of them, whose name is *DBUG*, because it only needs a serial port to connect the development station to *Antares* (the other one, *TUTOR* uses a BDM interface) and an in house developed monitor program, resident in the system non-volatile memory.

The modifications to the original monitor have imposed important changes in the application (because of the different commands and messages that the PC and *DAntares* exchange). Fortunately, there have been nonstructural ones because the operation philosophy is the same in both cases: during program execution and debugging a thread is in charge to monitor and to control the board.

In parallel to the modifications in the development toolkit, it has been necessary to also adapt the *DBUG* monitor modifying the memory map, initialization of the new devices, handling the flash memory, etc. The use of a Motorola evaluation board, used as reference, allowed us to parallelize the development of both HW and SW with remarkable success and reduction in development time.

The availability of the complete set of GNU tools for the C language allowed us to integrate them as scripts in the system to provide a high flexibility in programming and debugging. Although during the debug process, the assembler code is always visible (the student has to be conscious that the program is being executed on a physical machine and use the hardware

resources and special features by the inclusion of code in assembler), is possible to debug directly in C, track variables by the name (not only by address), etc.

VIII. Working experience with *DAntares*

The practical experience obtained up to now with the *Antares* and *DAntares* platforms both in education and in engineering are extremely good. A testing pack has been developed to monitor the system integrity both for validation and in house board maintenance, providing real merit figures. Testing software has two levels, at *CoLiLo* level it verifies the RAM memory, general purpose LED, RS232 interface, expansion bus, input/outputs (with an additional board), interruption and PWM lines, counters and system reset; and at *µCLinux* kernel level the USB, QSPI and Ethernet interfaces are tested.

The first pilot was carried out by a reduced workgroup in the *Laboratorio de Sistemas Electrónicos* to test the system in a real and controlled environment, previously to its implantation on the massive laboratory. The practice was an *mp3* player connected to an IP external server, using the *Antares* Web interface. The selected mp3 file had to be reproduced in *Antares* using the D/A converters. The experience was very positive both for the students and the Professors, validating the platform robustness and educational validity.

Actually new projects to develop hardware and software for the platform, including residential bridges and ICM networking for domotic applications are ongoing.

Other projects in the research, development and technology transfer activities are also being carrying ourt around this platform, as energy save system for buildings, greenhouses and extensive crops fertirrigation systems, systems to improve the Alzheimer illness quality of life, etc.

IX. Conclusions

The fruitful experience commented on this paper shows that cooperation between the R+D+I groups and the graduate education can be extremely productive in both senses. Graduate education improves with the state of the art technologies derived from the R+D+I groups and these ones can get better motivated and formed students for the future incorporation to the groups.

DAntares platform has been a complete success not only because it is a fully controlled and a state of the art microprocessor development system with in house maintenance capabilities, but also because the final price per equipment is less than buying commercial systems.

As conclusion of this fruitfully synergy, a new cooperation has started to afford the development of a new board that integrate *Antares* and an FPGA to cover the education on microprocessors, digital electronics and digital architectures.

Acknowledgement

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